What is claimed is:

1. A power-up circuit for use in a semiconductor memory device, comprising:

a power supply voltage level follower unit for outputting a first bias voltage and a second bias voltage which increase or decrease in proportion to a power supply voltage;

a first power supply voltage detecting unit for detecting a first critical voltage level where a logic level of a power-up signal is changed in response to the first bias voltage when the power supply voltage decreases;

a second power supply voltage detecting unit for detecting a second critical voltage level where a logic level of the power-up signal is changed in response to the second bias voltage when the power supply voltage increases; and

a trigger unit for inverting an output signal of the trigger unit in response to one of a first detect signal outputted from the first power supply voltage detecting unit when the power supply voltage decreases and a second detect signal outputted from the second power supply voltage detecting unit when the power supply voltage increases, wherein the second critical voltage level is higher than the first critical voltage level.

2. The power-up circuit as recited in claim 1, further includes a buffering unit for buffering an output signal from

the trigger unit to thereby output the power-up signal.

3. The power-up circuit as recited in claim 1, wherein the power supply voltage level follower unit includes a first load element, a second load element and a third load element all connected between the power supply voltage and a ground voltage for outputting the first bias voltage to a first common node between the first load element and the second load element and outputting the second bias voltage to a second common node between the second load element and the third load element.

4. The power-up circuit as recited in claim 1, wherein the first power supply voltage detecting unit includes:

a first load element connected between the power supply voltage and a first node;

a first NMOS transistor connected between the first node and a ground voltage for receiving the first bias voltage through a gate of the first NMOS transistor; and

a first inverter connected to the first node.

5. The power-up circuit as recited in claim 4, wherein the first load element is embodied as a PMOS transistor connected between the power supply voltage and the first node and a gate of the PMOS transistor is connected to the ground voltage.

6. The power-up circuit as recited in claim 4, wherein the second power supply voltage detecting unit includes:

a second load element connected between the power supply voltage and a second node;

a second NMOS transistor connected between the second node and the ground voltage for receiving the second bias voltage through a gate of the second NMOS transistor; and

a second inverter connected to the second node.

7. The power-up circuit as recited in claim 6, wherein the second load element is embodied as a PMOS transistor connected between the power supply voltage and the second node and a gate of the PMOS transistor is connected to the ground voltage.

8. The power-up circuit as recited in claim 1, wherein the trigger unit includes:

a pull-up unit controlled by the first detect signal; and

a pull-down unit controlled by the second detect signal.

9. The power-up circuit as recited in claim 6, wherein the trigger unit includes:

a PMOS transistor which is connected between the power supply voltage and a third node and receives the first detect signal through a gate of the PMOS transistor; and

a third NMOS transistor which is connected between the

ground voltage and the third node and receives the second detect signal through a gate of the third NMOS transistor.

10. The power-up circuit as recited in claim 9, wherein the trigger unit further includes a latch unit connected to the third node.

11. A power-up circuit for use in a semiconductor memory device, comprising:

a power supply voltage level follower unit for outputting a bias voltage which increases or decreases in proportion to a power supply voltage;

a first power supply voltage detecting unit for detecting a first critical voltage level where a logic level of a power-up signal is changed in response to the bias voltage when the power supply voltage decreases;

a second power supply voltage detecting unit for detecting a second critical voltage level where a logic level of the power-up signal is changed in response to the bias voltage when the power supply voltage increases; and

a trigger unit for inverting an output signal of the trigger unit in response to one of a first detect signal outputted from the first power supply voltage detecting unit when the power supply voltage decreases and a second detect signal outputted from the second power supply voltage detecting unit when the power supply voltage increases, wherein the second critical voltage level is higher than the

first critical voltage level.

12. The power-up circuit as recited in claim 11, further includes a buffering unit for buffering an output signal from the trigger unit to thereby output the power-up signal.

13. The power-up circuit as recited in claim 11, wherein the power supply voltage level follower unit includes a first load element and a second load element connected between the power supply voltage and a ground voltage for a voltage division.

14. The power-up circuit as recited in claim 11, wherein the first power supply voltage detecting unit includes:

a first load element connected between the power supply voltage and a first node;

a first NMOS transistor connected between the first node and a ground voltage for receiving the bias voltage through a gate of the first NMOS transistor; and

a first inverter connected to the first node.

15. The power-up circuit as recited in claim 14, wherein the first load element is embodied as a PMOS transistor connected between the power supply voltage and the first node and a gate of the PMOS transistor is connected to

the ground voltage.

16. The power-up circuit as recited in claim 14, wherein the second power supply voltage detecting unit includes:

a second load element connected between the power supply voltage and a second node;

a second NMOS transistor connected between the second node and the ground voltage for receiving the bias voltage through a gate of the second NMOS transistor; and

a second inverter connected to the second node, wherein a width of the second NMOS transistor is narrower than that of the first NMOS transistor.

17. The power-up circuit as recited in claim 14, wherein the second power supply voltage detecting unit includes:

a second load element connected between the power supply voltage and a second node;

a second NMOS transistor connected between the second node and the ground voltage for receiving the bias voltage through a gate of the second NMOS transistor; and

a second inverter connected to the second node, wherein a valid resistance of the second load element is less than that of the first load element.

18. The power-up circuit as recited in claim 16,

wherein the second load element is embodied as a PMOS transistor connected between the power supply voltage and the second node and a gate of the PMOS transistor is connected to the ground voltage.

19. The power-up circuit as recited in claim 17, wherein the second load element is embodied as a PMOS transistor connected between the power supply voltage and the second node and a gate of the PMOS transistor is connected to the ground voltage.

20. The power-up circuit as recited in claim 11, wherein the trigger unit includes:

a pull-up unit controlled by the first detect signal; and

a pull-down unit controlled by the second detect signal.

21. The power-up circuit as recited in claim 16, wherein the trigger unit includes:

a PMOS transistor which is connected between the power supply voltage and a third node and receives the first detect signal through a gate of the PMOS transistor; and

a third NMOS transistor which is connected between the ground voltage and the third node and receives the second detect signal through a gate of the third NMOS transistor.

22. The power-up circuit as recited claim 17, wherein

the trigger unit includes:

a PMOS transistor which is connected between the power supply voltage and a third node and receives the first detect signal through a gate of the PMOS transistor; and

a third NMOS transistor which is connected between the ground voltage and the third node and receives the second detect signal through a gate of the third NMOS transistor.

23. The power-up circuit as recited in claim 21, wherein the trigger unit further includes a latch unit connected to the third node.

24. The power-up circuit as recited in claim 22, wherein the trigger unit further includes a latch unit connected to the third node.